I, the undersigned, who have prepared English translation which is attached herewith, hereby declare that the aforementioned translation is true and correct translation of officially certified copy of the Korean Patent Application No. 10-2003-0021313 filed on April 4, 2003.

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(Translation)

APPLICATION FOR PATENT

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TITLE OF INVENTION: MULTI-DOMAIN LIQUID CRYSTAL DISPLAY AND A THIN FILM TRANSISTOR SUBSTRATE OF THE SAME

Submitted herewith is/are an application identified above pursuant to Article 42 of the Patent Act.

This 4th day of April, 2003

To the Commissioner of
the Korean Industrial Property Office

KOREAN INDUSTRIAL PROPERTY OFFICE

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Application Number: Patent Application No. 10-2003-0021313

Date of Application: April 4, 2003

Applicant(s): SAMSUNG ELECTRONICS CO., LTD.

COMMISSIONER

[ABSTRACT OF THE DISCLOSURE]

[ABSTRACT]

An embodiment of the present invention provides a thin film transistor array panel comprising: an insulating substrate; a first signal line formed on the insulating substrate and extending in a horizontal direction; a second signal line having a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, formed on the insulating substrate and intersecting the first signal line; a pixel electrode formed in each of pixel areas defined by intersection of the first and second signal lines; a thin film transistor connected to the first signal line, the second signal line and the pixel electrode, wherein the oblique portion connects between the longitudinal portions, the oblique portions include a first and a second oblique portions that are divided according to extending direction and wherein the second signal line deviates from a straight line due to the first oblique portion and the second signal line returns to the straight line due to the second oblique portion.

[REPRESENTATIVE FIGURE]

Fig. 1

[KEY WORDS]

liquid crystal display, domain, bent data line, thin film transistor array panel

[SPECIFICATION]

[TITLE OF THE INVENTION]

MULTI-DOMAIN LIQUID CRYSTAL DISPLAY AND A THIN FILM TRANSISTOR SUBSTRATE OF THE SAME

[BRIEF DESCRIPTION OF THE DRAWINGS]

Fig. 1 is a layout view of an LCD according to an embodiment of the present invention;

Fig. 2 is a sectional view of the LCD shown in Fig. 1 taken along the line II-II';

Fig. 3 is a sectional view of the LCD shown in Fig. 1 taken along the lines III-III' and III'-III";

Figs. 4A and 4B are sectional views of the TFT array panel shown in Figs. 1-3 taken along the line II-II' and the lines III-III' and III'-III", respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention;

Figs. 5A and 5B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 4A and 4B;

Fig. 6 is a layout view of an LCD according to another embodiment of the present invention;

Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along the line VII-VII';

Fig. 8 is a sectional view of the LCD shown in Fig. 6 taken along the lines VIII-VIII' and VIII'-VIII";

Figs. 9A and 9B are sectional views of the TFT array panel shown in Figs. 6-8 taken along the line VII-VII' and the lines VIII-VIII' and VIII'-VIII", respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention;

Figs. 10A and 10B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 9A and 9B;

Figs. 11A and 11B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 10A and 10B;

Figs. 12 and 13 are sectional views of the LCD shown in Fig. 1 according to another embodiment of the present invention;

Figs. 14 and 15 are sectional views of the LCD shown in Fig. 6 according to another embodiment of the present invention;

Figs. 16 and 17 are sectional views of the LCD shown in Fig. 1 according to another embodiment of the present invention; and

Figs. 18 and 19 are sectional views of the LCD shown in Fig. 6 according to another embodiment of the present invention.

[DETAILED DESCRIPTION OF THE INVENTION]

[OBJECT OF THE INVENTION]

[FIELD OF THE INVENTION AND CONVENTIONAL ART IN THE FIELD]

The present invention relates to a liquid crystal display and a thin film transistor array panel therefor.

A liquid crystal display (LCD) is one of the most widely used flat panel displays. An LCD includes two panels provided with field-generating electrodes and a liquid crystal (LC) layer interposed therebetween. The LCD displays images by applying voltages to the field-generating electrodes to generate an electric field in the LC layer, which determines orientations of LC molecules in the LC layer to adjust polarization of incident light.

The LCD has a narrow viewing angle. Various techniques for enlarging the viewing angle are suggested and a technique utilizing a vertically aligned LC and providing cutouts or protrusions at the field-generating electrodes such as pixel electrodes and a common electrode is promising.

Since the cutouts and the protrusions reduce the aperture ratio, it is required to reduce the area occupied by the cutouts and the protrusions. However, the width of the cutouts and the protrusions may be larger than a predetermined value and the distance of the cutouts and the protrusion may be smaller than a predetermined value in order to obtain stable LC domains defined by the cutouts and the protrusions and low response time of the LC.

[TECHNICAL TASK OF THE INVENTION]

It is an object of the present invention to provide a liquid crystal display which has a stable domain and high response speed and utmost aperture ratio.

[CONFIGURATION AND OPERATION of the invention]

An embodiment of the present invention provides a thin film transistor array panel comprising: an insulating substrate; a first signal line formed on the insulating substrate and extending in a horizontal direction; a second signal line having a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, formed on the insulating substrate and

intersecting the first signal line; a pixel electrode formed in each of pixel areas defined by intersection of the first and second signal lines; a thin film transistor connected to the first signal line, the second signal line and the pixel electrode, wherein the oblique portion connects between the longitudinal portions, the oblique portions include a first and a second oblique portions that are divided according to extending direction and wherein the second signal line deviates from a straight line due to the first oblique portion and the second signal line returns to the straight line due to the second oblique portion.

The first oblique portion may make a counterclockwise angle of about 45 degrees with the first signal line and the second oblique portion may make a clockwise angle of about 45 degrees with the first signal line.

The thin film transistor array panel further comprise a third signal line extending in the first direction and an electrode connected to the third signal line and bend along the second signal line.

The pixel electrode may have a side adjacent to the second signal line and may be bent along the second signal line.

An embodiment of the present invention provides a thin film transistor array panel comprising: an insulating substrate; a gate wire having a gate line and a gate electrode and formed on the insulating substrate; a gate insulating layer formed on the gate wire; a semiconductor layer formed on the gate insulating layer; a data wire formed on the insulating substrate and intersecting the first signal line and having a data line including a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, a source electrode connected to the data line, and a drain electrode facing the drain electrode on the gate electrode; a first passivation layer formed on the data wire; a pixel electrode formed on the first passivation layer, electrically connected to the drain electrode, and having a side adjacent to the data line and bent along the data line; a thin film transistor connected to the first signal line, the second signal line and the pixel electrode, wherein the oblique portions include a first and a second oblique portions that are divided according to extending direction and wherein the data line deviates from a straight line due to the first oblique portion and the data line returns to the straight line due to the second oblique portion.

The first oblique portion may make a counterclockwise angle of about 45 degrees with the gate line and the second oblique portion may make a clockwise angle of about 45 degrees with the gate line.

The thin film transistor array panel may further comprise a storage line extending in the first direction and an electrode connected to the storage line and bend along the data line.

The first passivation layer may be made of an organic insulating layer.

The first passivation layer may be formed of a photosensitive material by exposure to a light and development.

The first passivation layer may be made of an inorganic material and further comprising a color filter formed on the first passivation layer.

The color filter may include a red, a green and a blue color filters extending along a pixel column divided by the data line and the red, green and blue color filters may be arranged in turns.

The pixel electrode may be connected to the drain electrode through a contact hole penetrating the first passivation layer and a color filter removed area.

The portion around the contact hole of the first passivation layer may be exposed through the color filter removed area.

The thin film transistor array panel may further comprise first and second contact assistants connected to an ends of the gate line and the data line and made of the same material as the pixel electrode.

The thin film transistor array panel may further comprise a second passivation layer formed on the color filter and made of a photosensitive organic material.

The pixel electrode may be connected to the drain electrode through the first and second contact holes and the lateral side of the contact hole may make an angle of 30 degrees to 85 degrees with the insulating substrate.

The pixel electrode may be connected to the drain electrode through a contact hole penetrating the first and second passivation layer and the contact hole may have a step like profile.

The semiconductor layer may have a portion under the data line having substantially the same planar shape and a channel portion disposed under the source and drain electrode and their around.

An embodiment of the present invention provides a liquid crystal display comprising: a first insulating substrate; a first signal line formed on the first insulating substrate and extending in a horizontal direction; a second signal line having a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, formed on the first insulating substrate and intersecting the first signal line; a pixel electrode formed in each of pixel areas defined by intersection of the first and second signal lines; a thin film transistor connected to the first signal line, the second signal line and the pixel electrode, a second insulating substrate facing the first insulating substrate; a common electrode formed on the second insulating substrate; a domain dividing member formed at least one of the first and second insulating substrate; a liquid crystal layer interposed between the first and second insulating substrates; wherein the pixel area divided into a plurality of domains by the domain dividing member and each domain has two long sides parallel to the adjacent oblique portion and the longitudinal portions are parallel to a portion of the short sides of the domain.

The liquid crystal layer may have liquid crystals having negative dielectric constant and having long axis aligned in vertical to the first and second substrate.

The domain dividing members may be apertures that the common electrode and the pixel electrode have.

A liquid crystal is injected into the gap between the first and second substrates.

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. The present invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein.

In the drawings, the thickness of layers, films and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an element such as a layer, film, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

Now, TFT array panels and manufacturing methods thereof according to embodiments of the present invention will be described with reference to the accompanying drawings.

Fig. 1 is a layout view of an LCD according to an embodiment of the present invention, Fig. 2 is a sectional view of the LCD shown in Fig. 1 taken along the line II-II', and Fig. 3 is a sectional view of the LCD shown in Fig. 1 taken along the lines III-III' and III'-III".

An LCD according to an embodiment of the present invention includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed between the panels 100 and 200 and containing a plurality of LC molecules aligned vertical to surfaces of the panels 100 and 200.

The TFT array panel 100 is now described in detail.

A plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on an insulating substrate 110.

The gate lines 121 extend substantially in a transverse direction and are separated from each other and transmit gate signals. A plurality of projections of each gate line 121 form a plurality of gate electrodes 123. Each gate line 121 has an expansion 125 for contact with another layer or an external device.

Each storage electrode line 131 extends substantially in the transverse direction and it includes a plurality of sets of storage electrodes including a pair of longitudinal storage electrodes 133a and 133b and a transverse storage electrode 133c connecting the curved storage electrodes 133a and 133b, and a plurality of connectors 133d connecting two storage electrodes 133a and 133b in two neighboring sets of storage electrodes 133a-133c. The longitudinal storage electrodes 133a and 133b periodically curve and each of the longitudinal storage electrodes 133a has a free end portion and a fixed end portion connected to the storage electrode line 131, and both of the end portions have inclined edges. Each of the longitudinal storage electrodes 133a has two end portions, one connected to the storage electrode line 131 and the other connected to the connector 133d. The storage electrode lines 131 are supplied with a predetermined voltage such as a common voltage, which is applied to a common electrode 270 on the other panel 200 of the LCD.

The gate lines 121 as well as the storage electrode lines 131 include two films having different physical characteristics, a lower film 211 and an upper film 212. The upper film 212 is preferably made of low resistivity metal including Al containing metal such as Al and Al alloy for reducing signal delay or voltage drop in the gate lines 121 and the storage electrode lines 131. On the other hand, the lower film 211 is preferably made of material such as Cr, Mo and Mo

alloy, which has good contact characteristics with other materials such as indium tin oxide (ITO) or indium zinc oxide (IZO). A good exemplary combination of the lower film material and the upper film material is Cr and Al-Nd alloy. In Figs. 2 and 3, the lower and the upper films of the gate electrodes 123 are indicated by reference numerals 231 and 232, respectively, the lower and the upper films of the expansions 125 of the gate lines 121 are indicated by reference numerals 251 and 252, respectively, the lower and the upper films of the curved storage electrodes 133a are indicated by reference numerals 331a and 332a, respectively, and the lower and the upper films of the curved storage electrodes 133b are indicated by reference numerals 331b and 332b, respectively. Portions of the upper films 352 of the expansions 125 of the gate lines 121 are removed to expose the underlying portions of the lower films 351.

The gate lines 121 and the storage electrode lines 131 may have a single layered or multi-layered (i.e., triple or more layered) structure.

In addition, the edge surfaces of the gate lines 121 and the storage electrode lines 131 are tapered, and the inclination angle of the edge surfaces with respect to a surface of the substrate 110 ranges about 30-80 degrees.

A gate insulating layer 140 preferably made of silicon nitride (SiNx) is formed on the gate lines 121 and the storage electrode lines 131.

A plurality of semiconductor stripes 151 preferably made of hydrogenated amorphous silicon (abbreviated to "a-Si") are formed on the gate insulating layer 140. Each semiconductor stripe 151 extends substantially in the longitudinal direction while it is curved periodically. Each semiconductor stripe 151 has a plurality of projections 154 branched out toward the gate electrodes 123. The width of each semiconductor stripe 151 becomes large near the gate lines 121 such that the semiconductor stripe 151 covers large areas of the gate lines 121.

A plurality of ohmic contact stripes and islands 161 and 165 preferably made of silicide or n+ hydrogenated a-Si heavily doped with n type impurity are formed on the semiconductor stripes 151. Each ohmic contact stripe 161 has a plurality of projections 163, and the projections 163 and the ohmic contact islands 165 are located in pairs on the projections 154 of the semiconductor stripes 151.

The edge surfaces of the semiconductor stripes 151 and the ohmic contacts 161 and 165 are tapered, and the inclination angles of the edge surfaces of the semiconductor stripes 151 and the ohmic contacts 161 and 165 are preferably in a range between about 30-80 degrees.

A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.

The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121 to define pixel areas arranged in a matrix. Each data line 171 curves periodically and includes a plurality of sets of five longitudinal portions and four oblique portions connected between the longitudinal portions. Upper two of the four oblique portions make a counterclockwise angle of about 45 degrees with the gate lines 121, and lower two of the four oblique portions make a clockwise angle of about 45 degrees with the gate lines 121. Therefore, the data lines 171 step toward the left side, and then they return stepwise to their initial positions.

Therefore, each pixel area has a shape of a multi-bent band. The curvature of the semiconductor strips 151 and the ohmic contact stripes 161 overlapping the data lines 171 follows that of the data lines 171. Furthermore, the curve of the curved storage electrodes 133a and 133b also follows that of the data lines 171.

Each data line 171 includes an expansion 179 having wider width for contact with another layer or an external device. A plurality of branches of each data line 171, which project toward the drain electrodes 175, form a plurality of source electrodes 173. Each pair of the source electrodes 173 and the drain electrodes 175 are separated from each other and opposite each other with respect to a gate electrode 123. A gate electrode 123, a source electrode 173, and a drain electrode 175 along with a projection 154 of a semiconductor stripe 151 form a TFT having a channel formed in the projection 154 disposed between the source electrode 173 and the drain electrode 175.

The data lines 171 and the drain electrodes 175 also include a lower film 711, and 751 preferably made of Mo, Mo alloy or Cr and an upper film 712, and 752 located thereon and preferably made of Al containing metal or Ag containing metal. In Figs. 2 and 3, the lower and the upper films of the source electrodes 173 are indicated by reference numerals 731 and 732, respectively, and the lower and the upper films of the expansions 179 of the data lines 171 are indicated by reference numerals 791 and 792, respectively. Portion of the upper films 792, 752 of the expansions 179 of the data lines 171 and the drain electrodes 175 are removed to expose the underlying portions of the lower films 791 and 751.

Like the gate lines 121, the lower films 711, and 751 and the upper films 712 and 752 of the data lines 171 and the drain electrodes 175 have tapered edge surfaces, and the inclination angles of the edge surfaces range about 30-80 degrees.

A passivation layer 180 preferably made of organic insulator such as a photosensitive material is formed on the data lines 171 and the drain electrodes 175. The passivation layer 180 made of a photosensitive material can be patterned by exposure and development without etching process. Alternatively, the passivation layer 180 may be made of a photo-insensitive organic material or an inorganic material such as SiO_2 and SiNx.

The passivation layer 180 has a plurality of contact holes 181 and 183 exposing the lower films 751 of the drain electrodes 175 and the lower films 791 of the expansions 179 of the data lines 171, respectively. The passivation layer 180 and the gate insulating layer 140 have a plurality of contact holes 182, 184 and 185 exposing the expansions 125 of the gate lines 121, the free end portions of the first storage electrodes 133a, and portions of the storage electrode lines 131 near the fixed end portions of the first storage electrodes 133a, respectively. The sidewalls of the contact holes 181, 182, 183 as well as the contact holes 184 and 185 make an angle of about 30-85 degrees with respect to the surface of the substrate 110 and have stepped profiles including lower stairs 181b, 182b and 183b and upper stairs 181a, 182a and 183a as shown in Figs. 2 and 3.

The contact holes 181-185 may have a various planar shape such as rectangle and circle.

A plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91, which are preferably made of ITO or IZO, are formed on the passivation layer 180.

The pixel electrodes 190 are physically and electrically connected to the drain electrodes 175 through the contact holes 181 such that the pixel electrodes 190 receive the data voltages from the drain electrodes.

Each pixel electrode 190 has a shape of a multi-bent band following that of the pixel area. Each of the pixel electrodes 190 has a transverse cutout 191 that divide the pixel electrode 190 into upper and lower portions.

The storage connecting bridges 91 cross over the gate lines 121 and physically and connect neighboring storage electrode lines 131 trough the contact holes 184 and 185. A

conductor piece (not shown) may be disposed under each storage connecting bridge 91. The storage connecting bridges 91 electrically connect all of the storage electrode lines 131 on the substrate 110. The storage lines 131 and the storage bridges 91 can be used for repairing defects of the gate lines 121 and the data lines 171. The conducting pieces may enhance electrical connection between the gate lines 121 and the storage connection bridge 91 when a laser beam is illuminated for repairing.

The description of the common electrode panel 200 follows.

A black matrix 220 for preventing light leakage is formed on an insulating substrate 210 such as transparent glass.

A plurality of red, green and blue color filters 230 are formed on the black matrix and the substrate 210 and they extend substantially along the columns of the pixel areas such that they periodically curve.

An overcoat 250 is formed on the color filters 230 and the black matrix 220. A common electrode 270 preferably made of transparent conductive material such as ITO and IZO is formed on the overcoat 250. The common electrode 270 has a plurality of cutouts 271.

Each of the cutouts 271 of the common electrode 270 is curved like an inequality sign (<) such that it obliquely partition each of the upper and the lower portions of the pixel electrodes 190 into two pieces. The cutout 271 has end portions that are elongated in the longitudinal direction.

The overcoat 250 prevents the color filters 230 from being exposed through the cutouts 271 of the common electrode 270 to contaminate the LC layer 3.

A homogeneous or homeotropic alignment layer (not shown) is coated on the common electrode 270.

A pair of polarizers (not shown) are provided on outer surfaces of the panels 100 and 200 such that their transmissive axes are crossed and one of the transmissive axes is parallel to the gate lines 121.

The LCD may further include at least one retardation film for compensating the retardation of the LC layer 3.

The LC molecules in the LC layer 3 are aligned such that their long axes are vertical to the surfaces of the panels 100 and 200. The liquid crystal layer 3 has negative dielectric anisotropy.

Upon application of a common voltage to the common electrode 270 and a data voltage to the pixel electrodes 190, an electric field substantially perpendicular to the surfaces of the panels 100 and 200 is generated. The LC molecules tend to change their orientations in response to the electric field such that their long axes are perpendicular to the field direction. In the meantime, the cutouts 271 of the common electrode 270 and the edges of the pixel electrodes 190 distort the electric field to have a horizontal component which determines the tilt directions of the LC molecules. The horizontal component of the electric field is perpendicular to the edges of the cutouts 271 and the edges of the pixel electrodes 190. Accordingly, four domains having different tilt directions are formed in the LC layer 3.

As described above, since the area occupied by the cutouts 191 and 271 is reduced, the aperture ratio of the LCD is increased.

Since the tilt directions of all domains make an angle of about 45 degrees with the gate lines 121, which are parallel to or perpendicular to the edges of the panels 100 and 200, and the 45-degree intersection of the tilt directions and the transmissive axes of the polarizers gives maximum transmittance, the polarizers can be attached such that the transmissive axes of the polarizers are parallel to or perpendicular to the edges of the panels 100 and 200 and it reduces the production cost.

The resistance increase of the data lines 171 due to the curving can be compensated by widening the data lines 171 since distortion of the electric field and increase of the parasitic capacitance due to the increase of the width of the data lines 171 can be compensated by maximizing the size of the pixel electrodes 190 and by adapting a thick organic passivation layer.

A method of manufacturing the TFT array panel shown in Figs. 1, 2 and 3 according to an embodiment of the present invention will be now described in detail.

Figs. 4A and 4B are sectional views of the TFT array panel shown in Figs. 1-3 taken along the line II-II' and the lines III-III' and III'-III", respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention, and Figs. 5A and 5B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 4A and 4B.

Referring to Figs. 4A and 4B, two conductive films, a lower conductive film and an upper conductive film are sputtered in sequence on an insulating substrate 110 such as

transparent glass and they are wet or dry etched in sequence to form a plurality of gate lines 121 and a plurality of storage electrode lines 131.

After sequential deposition of a gate insulating layer 140 having a thickness of about 1,500-5,000 Å, an intrinsic a-Si layer having a thickness of about 500-2,000 Å, and an extrinsic a-Si layer having a thickness of about 300-600 Å, the extrinsic a-Si layer and the intrinsic a-Si layer are photo-etched to form a plurality of extrinsic semiconductor stripes and a plurality of intrinsic semiconductor stripes 151 including a plurality of projections 154 on the gate insulating layer 140.

Two conductive films, a lower conductive film and an upper conductive film having a thickness of 1,500-3,000 Å are sputtered in sequence and they are patterned to form a plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175.

Thereafter, portions of the extrinsic semiconductor stripes, which are not covered with the data lines 171 and the drain electrodes 175 are removed to complete a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 and to expose portions of the intrinsic semiconductor stripes 151. Oxygen plasma treatment preferably follows thereafter in order to stabilize the exposed surfaces of the semiconductor stripes 151.

Referring to Figs. 5A and 5B, a passivation layer 180 made of a photosensitive organic insulator is coated and exposed through a photo-mask 500 having a plurality of transmissive areas 502 and a plurality of slit areas 501 disposed around the transmissive areas 502.

Accordingly, portions of the passivation layer 180 facing the transmissive areas 502 absorb the full energy of the light, while portions of the passivation layer 180 facing the slit areas 501 partially absorb the light energy.

Subsequently, the passivation layer 180 is developed to form a plurality of contact holes 181-185. Since the portions of the passivation layer 180 facing the transmissive areas 502 are removed to its full thickness, while the portions facing the slit areas 501 remain to have reduced thickness, the contact holes 181-185 have stepped profiles.

Next, exposed portions of the upper conductive films 752, 792 and 252 of the expansions 179 of the data lines 171, the drain electrodes 175, and the expansions 125 of the gate

lines 121 as well as the upper conductive films of the storage electrode lines 131 are removed by etching.

An ITO or IZO film is deposited to have a thickness of about 400 Å o about 500 Å and is photo-etched to form a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91.

A TFT array panel for an LCD according to another embodiment of the present invention will be described in detail with reference to Figs. 6 to 11B.

Fig. 6 is a layout view of an LCD according to another embodiment of the present invention, Fig. 7 is a sectional view of the LCD shown in Fig. 6 taken along the line VII-VII', and Fig. 8 is a sectional view of the LCD shown in Fig. 6 taken along the lines VIII-VIII' and VIII'-VIII''.

Referring to Figs. 6-8, an LCD according to this embodiment also includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed therebetween.

Layered structures of the panels 100 and 200 according to this embodiment are almost the same as those shown in Figs. 1-3.

Regarding the TFT array panel 100, a plurality of gate lines 121 including a plurality of gate electrodes 123 and a plurality of storage electrode lines 131 including a plurality of storage electrodes 133a-133c and a plurality of storage connectors 133d are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of contact holes 181-185 are provided at the passivation layer 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91 are formed on the passivation layer 180.

Regarding the common electrode panel 200, a plurality of red, green and blue color filters 230 and a black matrix 220 for preventing light leakage are formed on an insulating substrate 210. An overcoat 250 is formed on the color filters 230 and the black matrix 220, and a common electrode 270 is formed on the overcoat 250.

Different from the LCD shown in Figs. 1-3, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165, except for the projections 154 where TFTs are provided. In detail, the projections 154 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

Now, a method of manufacturing the TFT array panel shown in Figs. 6 to 8 according to an embodiment of the present invention will be described in detail.

Figs. 9A and 9B are sectional views of the TFT array panel shown in Fig. 6-8 taken along the line VII-VII' and the lines VIII-VIII' and VIII'-VIII", respectively, in an intermediate step of a manufacturing method thereof according to an embodiment of the present invention; Figs. 10A and 10B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 9A and 9B; and Figs. 11A and 11B are sectional views of the TFT array panel in the step of the manufacturing method following the step shown in Figs. 10A and 10B.

Referring to Figs. 9A and 9B, two conductive films, a lower conductive film and an upper conductive film are sputtered in sequence on an insulating substrate 110 such as transparent glass and they are wet or dry etched in sequence to form a plurality of gate lines 121 and a plurality of storage electrode lines 131.

Next, a gate insulating layer 140, an intrinsic a-Si layer 150, and an extrinsic a-Si layer 160 are sequentially deposited by CVD such that the layers 140, 150 and 160 bear thickness of about 1,500-5,000 Å, about 500-2,000 Å and about 300-600 Å, respectively. A conductive layer 170 including a lower film 701 and an upper film 702 is deposited by sputtering, and a photoresist film with the thickness of about 1-2 microns is coated on the conductive layer 170.

The photoresist film is exposed to light through an exposure mask 600 including slit areas 601, and developed such that the developed photoresist PR has a position dependent thickness. The photoresist shown in Figs. 9A and 9B includes a plurality of first to third portions with decreased thickness. The first portions are located on wire areas A2 and the second portions are located on channel areas C2, respectively, while the third portions located on remaining areas B2 are not illustrated in the figures since they have substantially zero thickness to expose underlying portions of the conductive layer 170.

The different thickness of the photoresist PR enables to selectively etch the underlying layers when using suitable process conditions. Therefore, a plurality of data lines 171 including a plurality of source electrodes 173, and a plurality of drain electrodes 175 as well as a plurality of ohmic contact stripes 161 including a plurality of projections 163, a plurality of ohmic contact islands 165 and a plurality of semiconductor stripes 151 including a plurality of projections 154 are obtained by a series of etching steps as shown in Figs. 11A and 11B.

For descriptive purpose, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the wire areas A2 are called first portions, portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the channel areas C2 are called second portions, and portions of the conductive layer 170, the extrinsic a-Si layer 160, and the intrinsic a-Si layer 150 on the remaining areas B2 are called third portions.

An exemplary sequence of forming such a structure is as follows:

(1) Removal of third portions of the conductive layer 170, the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150 on the wire areas A2;

(2) Removal of the second portions of the photoresist;

(3) Removal of the second portions of the conductive layer 170 and the extrinsic a-Si layer 160 on the channel areas C2; and

(4) Removal of the first portions of the photoresist.

Another exemplary sequence is as follows:

(1) Removal of the third portions of the conductive layer 170;

(2) Removal of the second portions of the photoresist;

(3) Removal of the third portions of the extrinsic a-Si layer 160 and the intrinsic a-Si layer 150;

(4) Removal of the second portions of the conductive layer 170;

(5) Removal of the first portions of the photoresist; and

(6) Removal of the second portions of the extrinsic a-Si layer 160.

The first example is described in detail.

At first, the exposed third portions of the conductive layer 170 on the remaining areas B2 are removed by wet etching or dry etching to expose the underlying third portions of the extrinsic a-Si layer 160. The dry etching may etch out the top portions of the photoresist PR.

Next, the third portions of the extrinsic a-Si layer 160 on the areas B2 and of the intrinsic a-Si layer 150 are removed preferably by dry etching and the second portions of the photoresist PR are removed to expose the second portions of the conductors 170. The removal of the second portions of the photoresist PR are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer 160 and of the intrinsic a-Si layer 150. A gas mixture of SF_6 and HCl or a gas mixture of SF_6 and O_2 can etch the a-Si layers 150 and 160 and the photoresist PR by nearly the same etching ratio. Residue of the second portions of the photoresist PR remained on the channel areas C2 is removed by ashing.

Next, the third portions of the extrinsic a-Si layer 160 on the areas B2 and of the intrinsic a-Si layer 150 are removed preferably by dry etching and the second portions of the photoresist PR are removed to expose the second portions of the conductors 170. The removal of the second portions of the photoresist PR are performed either simultaneously with or independent from the removal of the third portions of the extrinsic a-Si layer 160 and of the intrinsic a-Si layer 150. A gas mixture of SF_6 and HCl or a gas mixture of SF_6 and O_2 can etch the a-Si layers 150 and 160 and the photoresist PR by nearly the same etching ratio. Residue of the second portions of the photoresist PR remained on the channel areas C2 is removed by ashing.

The semiconductor stripes 151 are completed in this step.

Next, the second portions of the conductors 170 and the extrinsic a-Si layer 160 on the channel areas C2 as well as the first portion of the photoresist PR are removed.

Both the conductors 170 and the extrinsic a-Si 160 may be dry etched.

Alternatively, the conductors 170 are wet etched, while the extrinsic a-Si layer 160 is dry etched. Since the wet etch etches out lateral sides of the conductors 170, while the dry etch hardly etch out lateral sides of the extrinsic a-Si layer 160, step-wise lateral profiles are obtained. Examples of the gas mixtures are CF_4 and HCl and CF_4 and O_2, as described above. The latter gas mixture leaves uniform thickness of the intrinsic semiconductor stripes 151.

In this way, each conductor 170 is divided into a data line 171 and a plurality of drain electrodes 175 to be completed, and the extrinsic a-Si layer 160 is divided into an ohmic contact stripe 161 and a plurality of ohmic contact islands 165 to be completed.

Referring to Figs 11A and 11B, a passivation layer 180 made of a photosensitive organic insulator is coated and exposed through a photo-mask 900 having a plurality of transmissive areas 902 and a plurality of slit areas 901 disposed around the transmissive areas 902. Accordingly, portions of the passivation layer 180 facing the transmissive areas 902 absorb the full energy of the light, while portions of the passivation layer 180 facing the slit areas 901 partially absorb the light energy.

Subsequently, the passivation layer 180 is developed to form a plurality of contact holes 181-185. Since the portions of the passivation layer 180 facing the transmissive areas 702 are removed to its full thickness, while the portions facing the slit areas 701 remain to have reduced thickness, the contact holes 181-185 have stepped profiles.

The passivation layer 180 may be made of a photo-insensitive organic insulator or inorganic insulator having a low dielectric constant under 4. In this case, an additional etching step for forming the contact holes 181-185 is required.

Referring to Figs 6 to 8, exposed portions of the upper conductive films 752, 792 and 252 of the expansions 179 of the data lines 171, the drain electrodes 175, and the expansions 125 of the gate lines 121 as well as the upper conductive films of the storage electrode lines 131 are removed by etching..

A plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridge 91 are formed by depositing and photo-etching an ITO or IZO film having a thickness of about 400 Å to about 500 Å.

The etching of the IZO film may include wet etching using a Cr etchant such as $HNO_3/(NH_4)_2Ce(NO_3)_6/H_2O$, which does not erode the exposed Al portions of the data lines 171, the drain electrodes 175, the gate lines 121, and the storage electrode lines 131 through the contact holes 181-185. A preferred deposition temperature for minimizing the contact resistance ranges from room temperature to about 200°C. A sputtering target for depositing IZO preferably includes In_2O_3 and ZnO and the content of ZnO is preferably in a range about 15-20 atomic%.

Nitrogen, which can prevent the formation of metal oxides on the exposed portions of the drain electrodes 175, the gate lines 121, the data lines 171, and the storage electrode lines 131 through the contact holes 181-185, is preferably used for a pre-heating process before the deposition of the ITO film or the IZO film.

Figs. 12 and 13 are sectional views of the LCD shown in Fig. 1 according to another embodiment of the present invention.

Referring to Figs. 12 and 13, an LCD according to this embodiment also includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed therebetween.

Regarding a TFT array panel 100, a plurality of gate lines 121 including a plurality of gate electrodes 123 and a plurality of storage electrode lines 131 including a plurality of storage electrodes 133a-133c and a plurality of storage connectors 133d are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 including a plurality of source electrodes 173 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165 and the gate insulating layer 140.

A first passivation layer 801 preferably made of inorganic insulator such as SiNx is formed on the data lines 171 and the drain electrodes 175.

A plurality of red, green and blue color filters 230R, 230G and 230B is formed on the first passivation layer 801. The color filters 230R, 230G and 230B extend substantially along the columns of the pixel areas defined by the data lines 171 such that they curve periodically. The neighboring color filters 230R, 230G and 230B overlap each other on the data lines 171 to form hills. The color filters 230R, 230G and 230B are not provided near the drain electrodes 175 and a peripheral area which is provided with the expansions 125 and 179 of the gate lines 121 and the data lines 179.

A second passivation layer 802 preferably made of photosensitive organic material is formed on the color filters 230R, 230G and 230B. The second passivation layer 802 also forms hills when running over the hills formed by the color filters 230R, 230G and 230B. The second passivation layer 802 The overcoat 250 prevents the color filters 230 from being exposed through the cutouts 271 of the common electrode 270 to contaminate the LC layer 3 and it may be made of inorganic insulator such as SiNx and SiO_2.

The passivation layers 801 and 802 have a plurality of contact holes 181 and 183, and the passivation layers 801 and 802 and the gate insulating layer 140 have a plurality of contact holes 182, 184 and 185. The sidewalls of the contact holes 181, 182, 183 as well as the contact holes 184 and 185 make an angle of about 30-85 degrees with respect to the surface of the

substrate 110 and have stepped profiles including lower stairs 181b, 182b and 183b and upper stairs 181a, 182a and 183a.

A plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a storage connecting bridge 91 are formed on the second passivation layer 802.

The common electrode panel 200 includes a black matrix 220 and a common electrode 270 formed on an insulating substrate 210. Comparing the common electrode panel 200 shown in Figs. 2 and 3, the common electrode panel 200 shown in Fig. 12 and 13 has no color filter and no overcoat.

Since the color filters 230R, 230G and 230B and the pixel electrodes 190 are provided on the TFT array panel 100, the LCD shown in Figs. 12 and 13 may have a large alignment margin for aligning the TFT array panel 100 and the common electrode panel 200.

A TFT array panel 100 shown in Figs. 12 and 13 may be manufactured by depositing a first passivation layer 801, forming a plurality of red, green, and blue color filters 230R, 230G, and 230B, coating a second passivation layer 802 made of a photosensitive organic layer, exposing and developing the passivation layer 802 to form upper portions of a plurality of contact holes 181-185, removing exposed portions of the first passivation layer 801 and the gate insulating layer 140 to form lower portions of the contact holes 181-185, and forming a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91, after forming the gate lines 121, the storage electrode lines 131, the gate insulating layer 140, the semiconductor stripes 151, the ohmic contacts 161 and 165, the data lines 171, and the drain electrodes 175 as described above with reference to Figs. 1-4B. The formation of the color filters 230R, 230G, and 230B includes thrice repetitions of coating, exposing, and developing a photosensitive film including a colored pigment.

Many of the above-described features of the LCD shown in Figs. 1-3 may be appropriate to the LCD shown in Figs. 12 and 13.

Fig. 14 and 15 are sectional views of the LCD shown in Fig. 6 according to another embodiment of the present invention.

Referring to Figs. 14 and 15, an LCD according to this embodiment also includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed therebetween.

Layered structures of the panels 100 and 200 according to this embodiment are almost the same as those shown in Figs. 12 and 13.

Concerning the TFT array panel 100, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a first passivation layer 801 is formed thereon. A plurality of red, green and blue color filters 230 are formed on the first passivation layer 801 and a second passivation layer 802 is formed thereon. A plurality of contact holes 181-185 are provided at the first and the second passivation layers 801 and 802 and the gate insulating layer 140, and a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91 are formed on the second passivation layer 802.

Concerning the common electrode panel 200, a black matrix 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in Figs. 12 and 13, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165, except for the projections 154 where TFTs are provided. In detail, the projections 154 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

A TFT array panel 100 shown in Figs. 14 and 15 may be manufactured by forming a first passivation layer 801, a plurality of red, green, and blue color filters 230R, 230G, and 230B, a second passivation layer 802, a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91 based on the steps described with reference to Figs. 12 and 13, after forming the gate lines 121, the storage electrode lines 131, the gate insulating layer 140, the semiconductor stripes 151, the ohmic contacts 161 and 165, the data lines 171, and the drain electrodes 175 based on the steps described with reference to Figs. 6-10B.

Many of the above-described features of the LCD shown in Figs. 6-8 may be appropriate to the LCD shown in Figs. 14 and 15.

Figs. 16 and 17 are sectional views of the LCD shown in Fig. 1 according to another embodiment of the present invention.

Referring to Figs. 16 and 17, an LCD according to this embodiment also includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed therebetween.

Layered structures of the panels 100 and 200 according to this embodiment are almost the same as those shown in Figs. 12 and 13.

Concerning the TFT array panel 100, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230R, 230G, and 230B are formed on the passivation layer 801 and a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91 are formed on the second passivation layer 802. A plurality of contact holes 181-185 are provided at the passivation layer 180 and the gate insulating layer 140.

Concerning the common electrode panel 200, a black matrix 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in Figs. 12 and 13, there is no additional passivation layer on the color filters 230R, 230G, and 230B. Accordingly, lateral surfaces of the color filters 230R, 230G, and 230B near the contact holes 181, 184 and 185 serve as upper portions of sidewalls of the contact holes 181, 184 and 185 to smooth the profiles thereof as shown in Fig. 16. This structure is preferable when the color filters 230R, 230G and 230B do not discharge impurities such as pigment that may contaminate the LC layer 3.

Figs. 18 and 19 are sectional views of the LCD shown in Fig. 6 according to another embodiment of the present invention;

Referring to Figs. 18 and 19, an LCD according to this embodiment also includes a TFT array panel 100, a common electrode panel 200, and a LC layer 3 interposed therebetween.

Layered structures of the panels 100 and 200 according to this embodiment are almost the same as those shown in Figs. 16 and 17.

Concerning the TFT array panel 100, a plurality of gate lines 121 and a plurality of storage electrode lines 131 are formed on a substrate 110, and a gate insulating layer 140, a plurality of semiconductor stripes 151 including a plurality of projections 154, and a plurality of ohmic contact stripes 161 including a plurality of projections 163 and a plurality of ohmic contact islands 165 are sequentially formed thereon. A plurality of data lines 171 and a plurality of drain electrodes 175 are formed on the ohmic contacts 161 and 165, and a passivation layer 180 is formed thereon. A plurality of red, green and blue color filters 230 are formed on the passivation layer 180. A plurality of contact holes 181-185 are provided at the passivation layers 180 and the gate insulating layer 140, and a plurality of pixel electrodes 190, a plurality of contact assistants 95 and 97, and a plurality of storage connecting bridges 91 are formed on the passivation layer 180.

Concerning the common electrode panel 200, a black matrix 220 and a common electrode 270 are sequentially formed on an insulating substrate 210.

Different from the LCD shown in Figs. 16 and 17, the semiconductor stripes 151 have almost the same planar shapes as the data lines 171 and the drain electrodes 175 as well as the underlying ohmic contacts 161 and 165, except for the projections 154 where TFTs are provided. In detail, the projections 154 include some exposed portions, which are not covered with the data lines 171 and the drain electrodes 175 such as portions located between the source electrodes 173 and the drain electrodes 175.

While the present invention has been described in detail with reference to the preferred embodiments, those skilled in the art will appreciate that various modifications and substitutions can be made thereto without departing from the spirit and scope of the present invention as set forth in the appended claims.

[ADVANTAGE OF THE INVENTION]

As described above, when the data lines are formed to have a form of a multi-bent stripe, aperture ratio is improved. A polarizer may be disposed to have its transmission axis perpendicular or parallel to the gate line. Accordingly, the manufacturing cost of the polarizer may be reduced and the liquid crystals in every domain initially aligned to make an angle of 45degrees with the transmission axis of the polarizer.

[CLAIMS]

1. A thin film transistor array panel comprising:

an insulating substrate;

a first signal line formed on the insulating substrate and extending in a horizontal direction;

a second signal line having a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, formed on the insulating substrate and intersecting the first signal line;

a pixel electrode formed in each of pixel areas defined by intersection of the first and second signal lines;

a thin film transistor connected to the first signal line, the second signal line and the pixel electrode,

wherein the oblique portion connects between the longitudinal portions, the oblique portions include a first and a second oblique portions that are divided according to extending direction and wherein the second signal line deviates from a straight line due to the first oblique portion and the second signal line returns to the straight line due to the second oblique portion.

2. The thin film transistor array panel of claim 1, wherein the first oblique portion make a counterclockwise angle of about 45 degrees with the first signal line and the second oblique portion make a clockwise angle of about 45 degrees with the first signal line.

3. The thin film transistor array panel of claim 1, further comprising a third signal line extending in the first direction and an electrode connected to the third signal line and bend along the second signal line.

4. The thin film transistor array panel of claim 1, wherein the pixel electrode having a side adjacent to the second signal line and bent along the second signal line.

5. A thin film transistor array panel comprising:

an insulating substrate;

a gate wire having a gate line and a gate electrode and formed on the insulating substrate;

a gate insulating layer formed on the gate wire;

a semiconductor layer formed on the gate insulating layer;

a data wire formed on the insulating substrate and intersecting the first signal line and having a data line including a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, a source electrode connected to the data line, and a drain electrode facing the drain electrode on the gate electrode;

a first passivation layer formed on the data wire;

a pixel electrode formed on the first passivation layer, electrically connected to the drain electrode, and having a side adjacent to the data line and bent along the data line;

a thin film transistor connected to the first signal line, the second signal line and the pixel electrode,

wherein the oblique portions include a first and a second oblique portions that are divided according to extending direction and wherein the data line deviates from a straight line due to the first oblique portion and the data line returns to the straight line due to the second oblique portion.

6. The thin film transistor array panel of claim 5, wherein the first oblique portion make a counterclockwise angle of about 45 degrees with the gate line and the second oblique portion make a clockwise angle of about 45 degrees with the gate line.

7. The thin film transistor array panel of claim 5, further comprising a storage line extending in the first direction and an electrode connected to the storage line and bend along the data line.

8. The thin film transistor array panel of claim 5, wherein the first passivation layer is made of an organic insulating layer.

9. The thin film transistor array panel of claim 8, wherein the first passivation layer is formed of a photosensitive material by exposure to a light and development.

10. The thin film transistor array panel of claim 5, wherein the first passivation layer is made of an inorganic material and further comprising a color filter formed on the first passivation layer.

11. The thin film transistor array panel of claim 10, wherein the color filter includes a red, a green and a blue color filters extending along a pixel column divided by the data line and the red, green and blue color filters are arranged in turns.

12. The thin film transistor array panel of claim 10, wherein the pixel electrode is connected to the drain electrode through a contact hole penetrating the first passivation layer and a color filter removed area.

13. The thin film transistor array panel of claim 12, wherein the portion around the contact hole of the first passivation layer is exposed through the color filter removed area.

14. The thin film transistor array panel of claim 10, further comprising first and second contact assistants connected to an ends of the gate line and the data line and made of the same material as the pixel electrode.

15. The thin film transistor array panel of claim 10, further comprising a second passivation layer formed on the color filter and made of a photosensitive organic material.

16. The thin film transistor array panel of claim 15, wherein the pixel electrode connected to the drain electrode through the first and second contact holes and the lateral side of the contact hole make an angle of 30 degrees to 85 degrees with the insulating substrate.

17. The thin film transistor array panel of claim 15, wherein the pixel electrode connected to the drain electrode through a contact hole penetrating the first and second passivation layer and the contact hole has a step like profile.

18. The thin film transistor array panel of claim 5, wherein the semiconductor layer has a portion under the data line having substantially the same planar shape and a channel portion disposed under the source and drain electrode and their around.

19. A liquid crystal display comprising:

a first insulating substrate;

a first signal line formed on the first insulating substrate and extending in a horizontal direction;

a second signal line having a plurality of oblique portions and longitudinal portions repeatedly appearing in turns, formed on the first insulating substrate and intersecting the first signal line;

a pixel electrode formed in each of pixel areas defined by intersection of the first and second signal lines;

a thin film transistor connected to the first signal line, the second signal line and the pixel electrode,

a second insulating substrate facing the first insulating substrate;

a common electrode formed on the second insulating substrate;

a domain dividing member formed at least one of the first and second insulating substrate;

a liquid crystal layer interposed between the first and second insulating substrates;

wherein the pixel area divided into a plurality of domains by the domain dividing member and each domain has two long sides parallel to the adjacent oblique portion and the longitudinal portions are parallel to a portion of the short sides of the domain.

20. The thin film transistor array panel of claim 19, wherein the liquid crystal layer has liquid crystals having negative dielectric constant and having long axis aligned in vertical to the first and second substrate.

21. The thin film transistor array panel of claim 19, wherein the domain dividing members are apertures that the common electrode and the pixel electrode have.